Universidade Federal de Santa Catarina
Centro Tecnológico
Departamento de Informática e Estatística
Programa de Pós-Graduação em Ciência da Computação

Course Plan

1) Identification

Course: Electronic Design Automation (Automação do Projeto Eletrônico)
Workload: 60 horas-aula - 4 créditos
Instructor: Cristina Meinhardt and José Luís Güntzel
Semester: 2022.1

2) Prerequisites:

Knowledge of programming, data structures and digital design proved through undergraduate and/or graduate courses successfully followed.

3) Syllabus:

The Electronic Design Automation (EDA) design flow, fundamental algorithms, Electronic System-Level (ESL) design and High-Level Synthesis (HLS), Logic Synthesis (LS), verification and test, Physical Synthesis (PS), implementation issues on selected problems.

4) Course Objective

General:

Provide a broad view of the electronic design automation of contemporary VLSI circuits.

Specific Objectives:

- Present the different levels of abstraction of the representation of contemporary digital systems, relating them to the respective stages of synthesis and CMOS manufacturing technology;
- Provide an understanding of the characteristics and requirements of each step of digital circuit synthesis, presenting the usual formulations of each step;
- Present and discuss the most important algorithms and techniques for the various synthesis steps, possibly correlating the respective algorithms to the most appropriate data structures;
- Allow students to go into the details of a technique/algorithm related to one of the synthesis steps by implementing a prototype.

5) Contents:

- Contemporary VLSI design flow and typical Electronic Design Automation (EDA) flow.
- Basic CMOS gates, CMOS fabrication technology and design rules.
- Fundamental algorithms: Computational complexity, Graph algorithms, Heuristic algorithms and Mathematical programming.
- Electronic System-Level (ESL) Design and High-Level Synthesis (HLS):
    - ESL design methodologies;
    - Fundamentals of HLS;
    - Scheduling;
    - Register Biding;
    - Functional unit biding.

- Logic Synthesis (LS):
    - Data structure for Boolean representation;
    - Combinational logic minimization;
    - Technology mapping;
    - Timing analysis and optimization.
- Fault Simulation, Test Synthesis and Verification:
    - Fault models and fault simulation;
    - Test generation algorithms;
    - Design for testability techniques;
    - Simulation-based approach and formal approaches.
- Physical Synthesis (PS):
    - Basic PS concepts and standard cell-based design;
    - Netlist and system partitioning;
    - Chip planning;
    - Global and detailed placement;
    - Global routing;
    - Detailed routing;
    - Specialized routing;
    - Timing Closure.
- EDA practical aspects: prototype implementation of selected technique.

6) Methodology

The topics will be presented by the instructors by means of slides prepared based upon the course textbooks, tutorial materials, and a series of video courses about the EDA flow. The students are requested to make further readings in the textbooks, watch the videos, take notes, elaborate presentations, and actively participate in the discussions. This semester, the course will conduct 44% of the activities in an asynchronous mode, with material provided by video classes, discussion on forums and text references.
The course will also count with a practical part in which the student will be in contact with an Open EDA flow. The course contemplates the selection of state-of-art topics to be presented in a final seminar.

7) Assessment and Grading

The assessment instruments are:

EDA Flow Activities (EFA): elaboration of notes and presentations to discuss the EDA steps. The final grade for this activity will be determined by the arithmetic average of 11 activities completed in the semester.

Discussions (D): all the participants must actively participate in the discussion activities.

Implementation task (I): the students will select one topic to implement an algorithm, a part of an existing technique or propose a modification on a traditional technique.

Seminar (S): the students will select a state-of-art article for presentation and discussion.

The final grade (G) will be computed as:

$G = 0.4\ EFA + 0.2\ D + 0.2\ I + 0.2\ S$

8) Schedule

Class	Mode	Contents
1	Presential	Contemporary VLSI design flow and typical Electronic Design Automation (EDA) flow. − Basic CMOS gates, CMOS fabrication technology and design rules
2	Presential	− Fundamental algorithms, Computational complexity
3	Presential	Introduction to the Integrated Circuit Design
4	Asynchronous	Introduction to the Modern Design Flow
5	Presential	Discussion 1: Traditional versus Modern Design Flow
6	Asynchronous	Logic Synthesis (LS)
7	Presential	Discussion 2: Logic Synthesis Challenges
8	Asynchronous	Floorplanning
9	Presential	Discussion 3: Floorplanning Concepts
10	Asynchronous	Placement: Global Placement
11	Presential	Discussion 4: Global Placement Challenges
12	Asynchronous	Placement: Legalization and Detailed Placement
13	Presential	Discussion 5: Placement Challenges
14	Asynchronous	Routing: Global Routing
15	Presential	Discussion 6: Global Routing Techniques
16	Asynchronous	Routing: Detailed Routing
17	Presential	Discussion 7: Routing Challenges
18	Asynchronous	Practical Activities: Installing and Understanding the Open Road Flow
19	Presential	Classic Placement Algorithms and Data Structures
20	Asynchronous	Practical Activities: Installing and Understanding the Open Road Flow
21	Presential	Classic Routing Algorithms and Data Structures
22	Asynchronous	Timing closure/optimization and Gate Sizing
23	Presential	Discussion 8: Timing and Gate Sizing Optimization
24	Asynchronous	Clock Synthesis
25	Presential	Discussion 10: Algorithms for clock synthesis and challenges
26	Asynchronous	Automatic Cell Generation
27	Presential	Discussion 11: Automatic Cell Generation versus Standard Cell Flow
28	Asynchronous	Implementation task - development
29	Asynchronous	Implementation task - development
30	Presential	Seminar
31	Presential	Seminar
32	Presential	Implementation Presentations

9) Textbooks

[1] WANG, Laung-Terng ; CHANG, Yao-Wen ; CHENG, Kwang-Ting (Tim). Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon). Morgan Kaufmann. 1st edition (March 12, 2009) ISBN-10: 0123743648 ISBN-13: 978-0123743640 https://www.sciencedirect.com/science/book/9780123743640

[2] KAHNG, Andrew B.; LIENIG, Jens; MARKOV, Igor L.; HU, Jin. VLSI Physical Design: From Graph Partitioning to Timing Closure. Dordrecht: Springer, 2011. 310 p. ISBN-13: 978-9048195909

8) Complementary Bibliography

[3] CORMEN, Thomas H.; LEISERSON, Charles E.; RIVEST, Ronald L.; STEIN, Clifford. Introduction to Algorithms. The MIT Press; 3rd edition (July 31, 2009) ISBN-10: 0262033844 ISBN-13: 978-0262033848.

[4] WESTE, Neil; HARRIS, David. CMOS VLSI Design: a circuits and systems perspective. Addison-Wesley, 4th Edition, 2010. ISBN 978-0321547743.

[5] LAVAGNO, Luciano; MARKOV, Igor L.; MARTIN, Grant E.; SCHEFFER, Louis K. Electronic Design Automation for Integrated Circuits Handbook, Second Edition - (Two Volume Set). CRC Press; 2 edition (May 5, 2016) ISBN-10: 1482254506 ISBN-13: 978-1482254501

[6] De Micheli, Giovanni. Synthesis and Optimization of Digital Circuits. McGraw-Hill, 1994) ISBN-10: 0070163332 ISBN-13: 978-0070163331.

[7] MARTIN, Grant. ESL Design and Verification: a prescription for electronic system level methodology (Systems on Silicon) Morgan Kaufmann, 2007. 1st Edition. ISBN-10: 0123735513 ISBN-13: 978-0123735515

[8] WILE, Bruce, GOSS, John; ROESNER, Wolfgang. Comprehensive Functional Verification. Morgan Kaufmann, 2005.

[9] ALPERT, Charles J.; MEHTA, Dinesh P.; SAPATNEKAR, Sachin S. (Editors) Handbook of Algorithms for Physical Design Automation. [S.l.]: Auerbach Publications, 2008. 1024 p. ISBN-13: 978-0849372421

[10] LIM, Sung Kyu. Practical Problems in VLSI Physical Design Automation. Dordrecht: Springer; 2008. 264 p. ISBN-13: 978-1402066269

[11] Selected papers of state-of-the-art EDA techniques.